

MSI:MS-7245N1

NEC:(Babel)(MT3H)

Version 1.2

System Chipset:

Intel Broadwater - GMCH (North Bridge)

Intel ICH8(DO)(R) (South Bridge)

On Board Chipset:

BIOS -- SPI Flash 8Mb or 16Mb

HD AUDIO -- ALC262

LPC Super I/O -- SMSC--SHC5017

LAN -- Intel Neneveh 82566 DM/DC

IDE-- VIA VT-6410

CLOCK -- CY505YC64CT

Main Memory:

2 CHANNEL DDR II * 4 (Max 8GB)

Expansion Slots:

PCIE x16 SLOT * 1

PCIE x1 SLOT * 1

PCI SLOT * 1

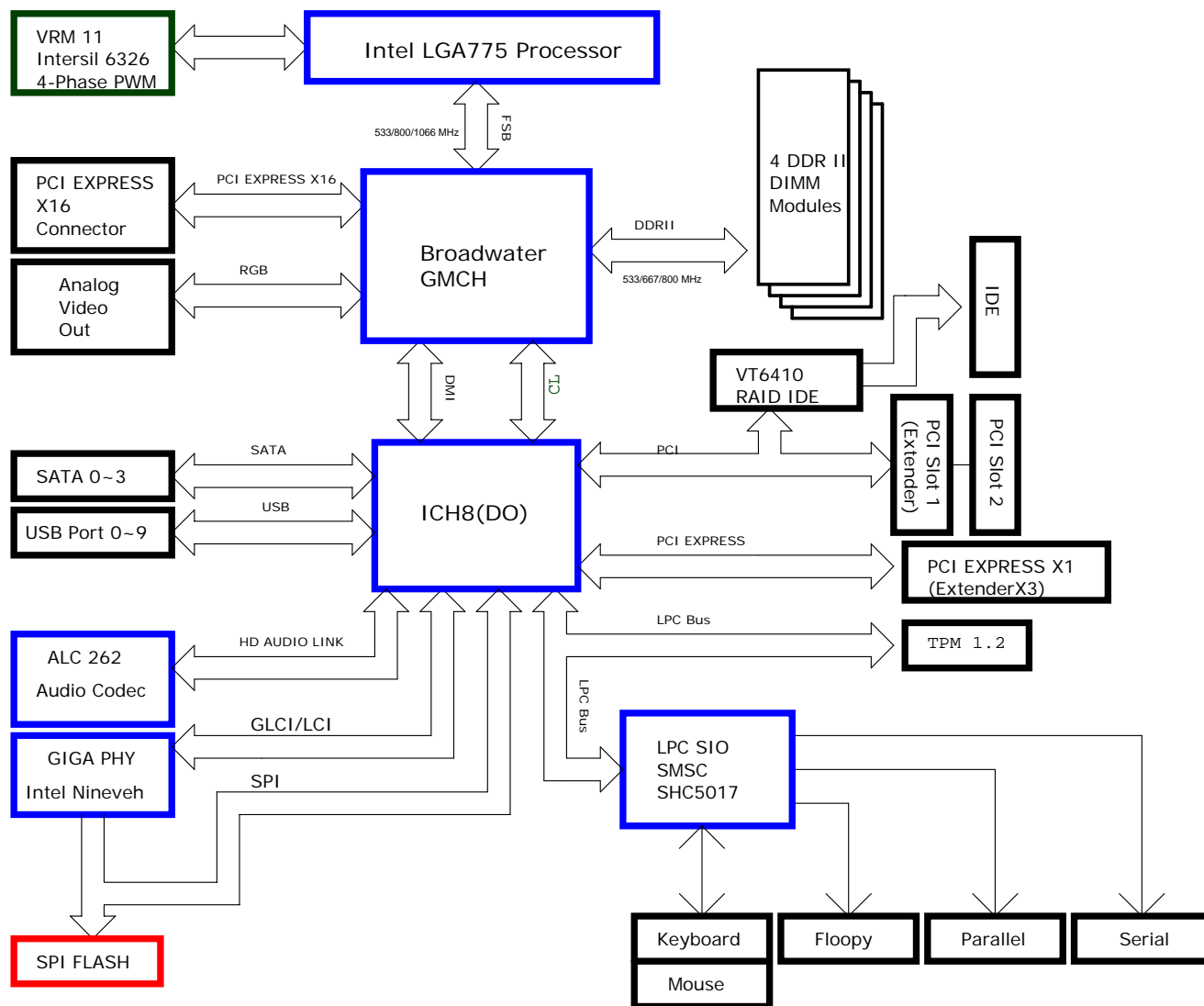
PCI(Extender)SLOT * 1

Intersil PWM:

Controller: INTERSIL 6326 4 PHASES

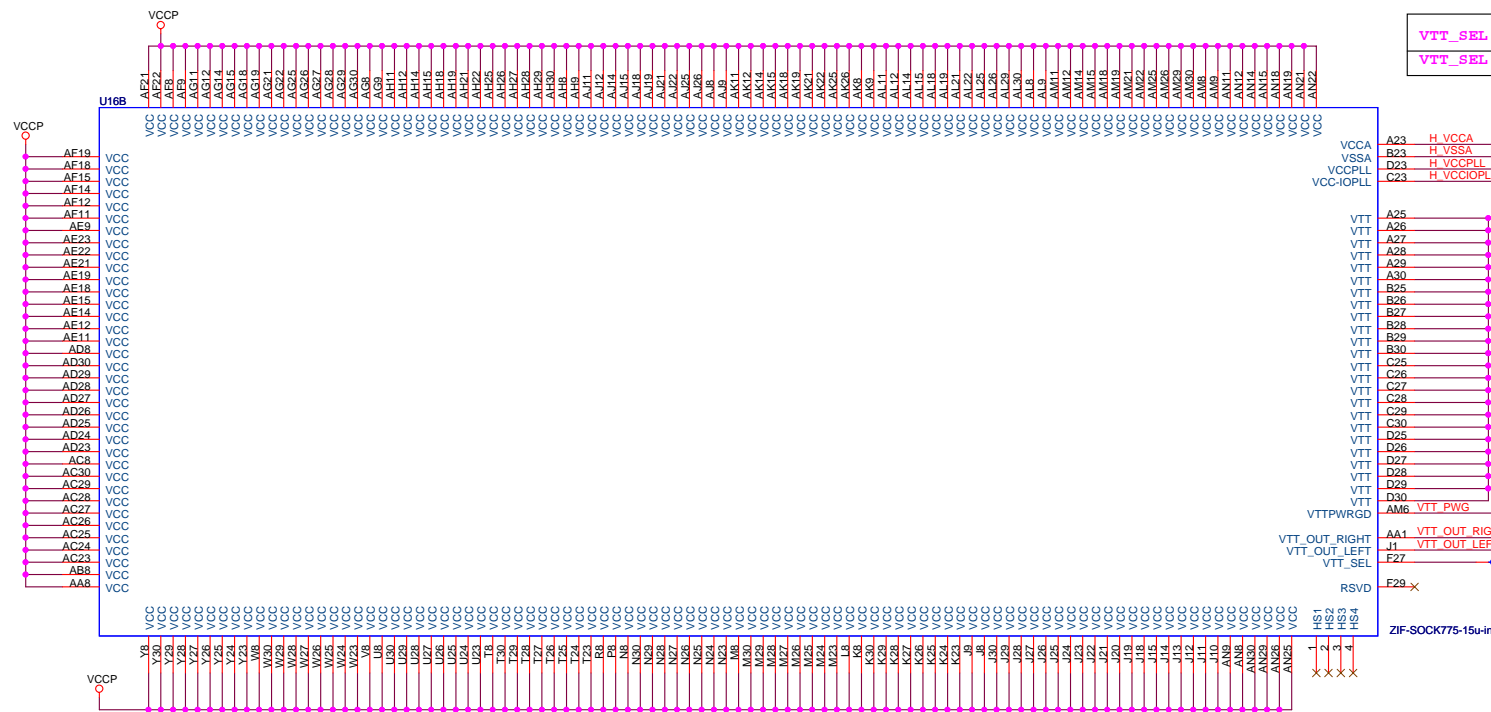
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Block Diagram

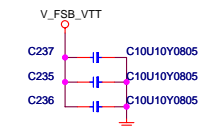


[illegible]

BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

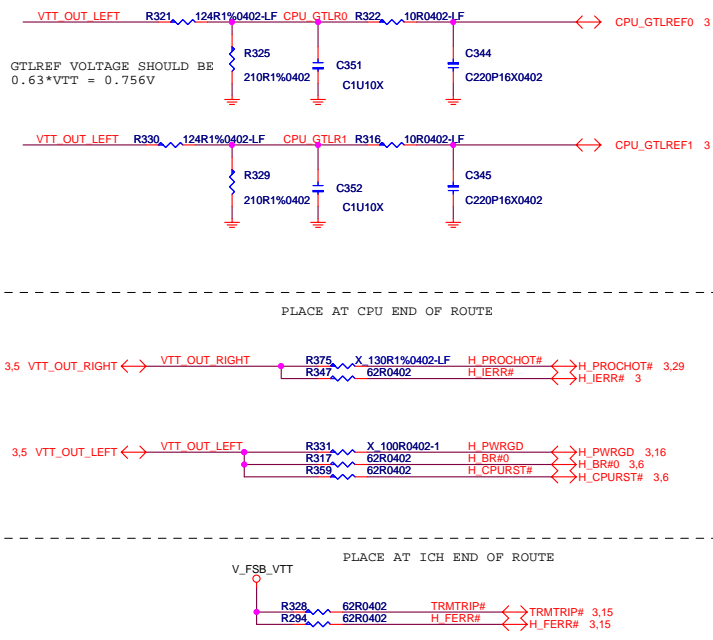


VTT_SEL = H	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = L	V_FSB_VTT=1.2V	For normal processors.



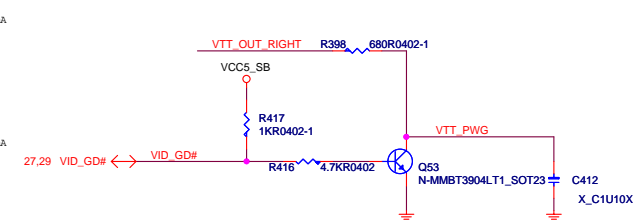
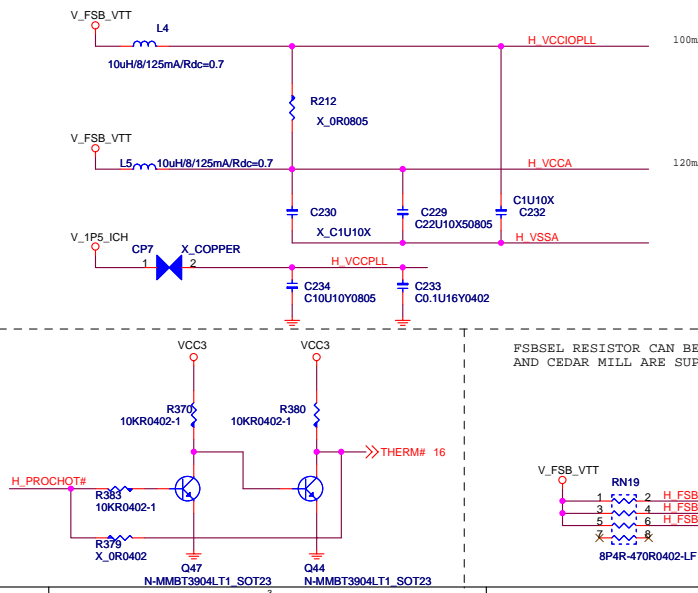
CAPS FOR FSB GENERIC

LGA775 pin AM6 is VTT_PWRGD, But for Conroe, AM6 is a reserved pin.(VTT_PWRGD didn't exist on Conroe.)

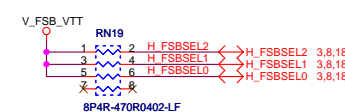


PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS

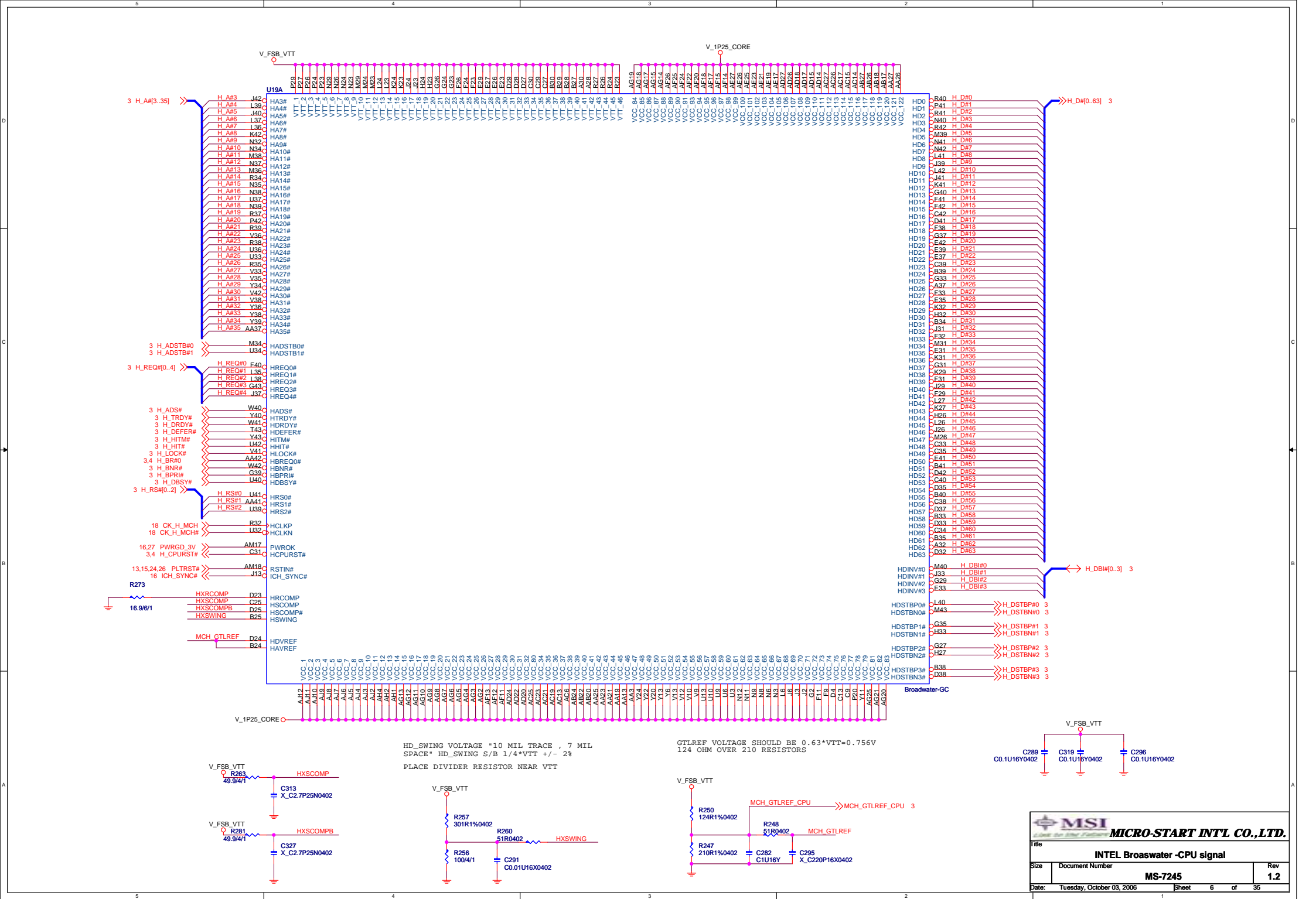
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns

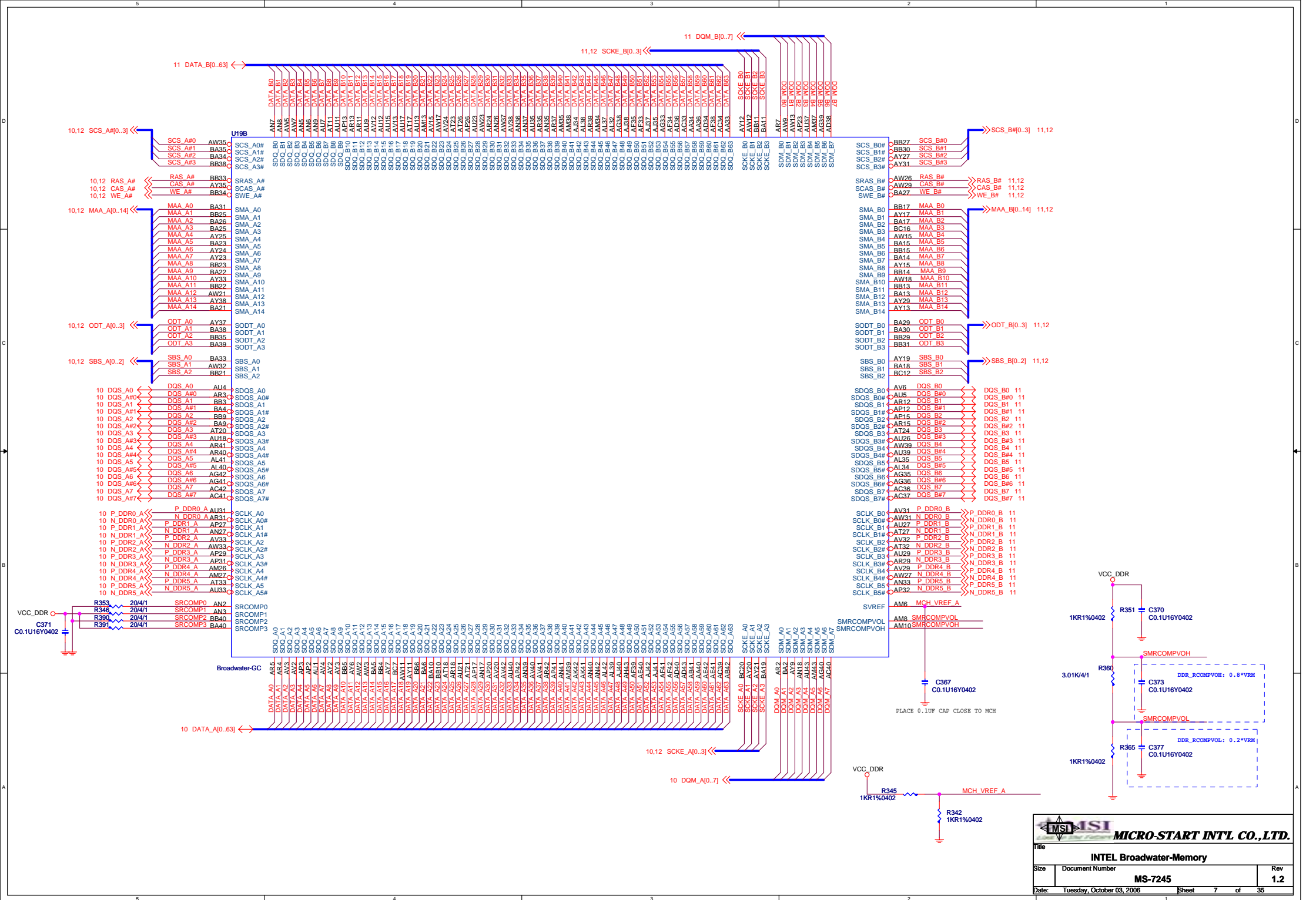


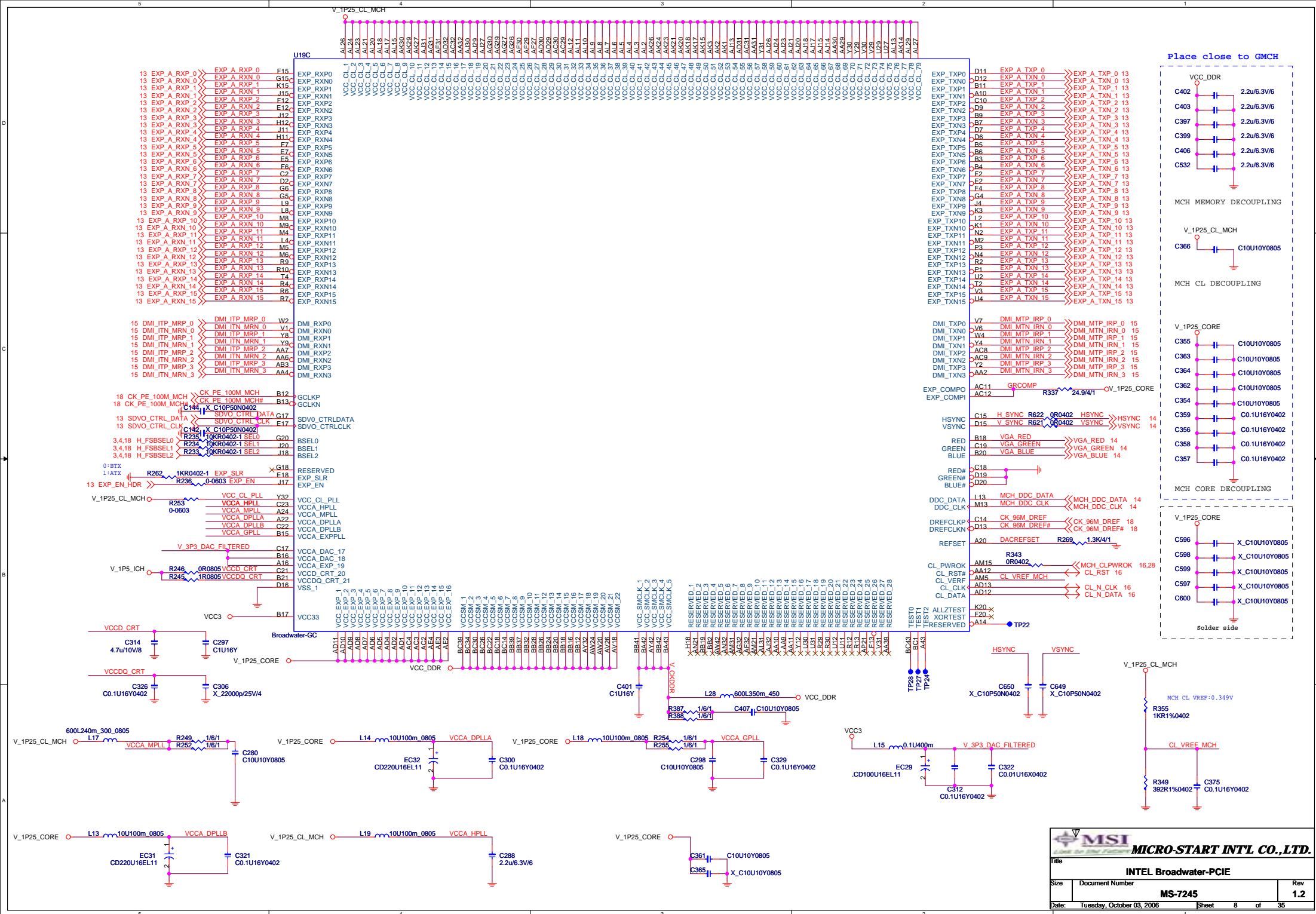
FSBSEL RESISTOR CAN BE REMOVED IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED



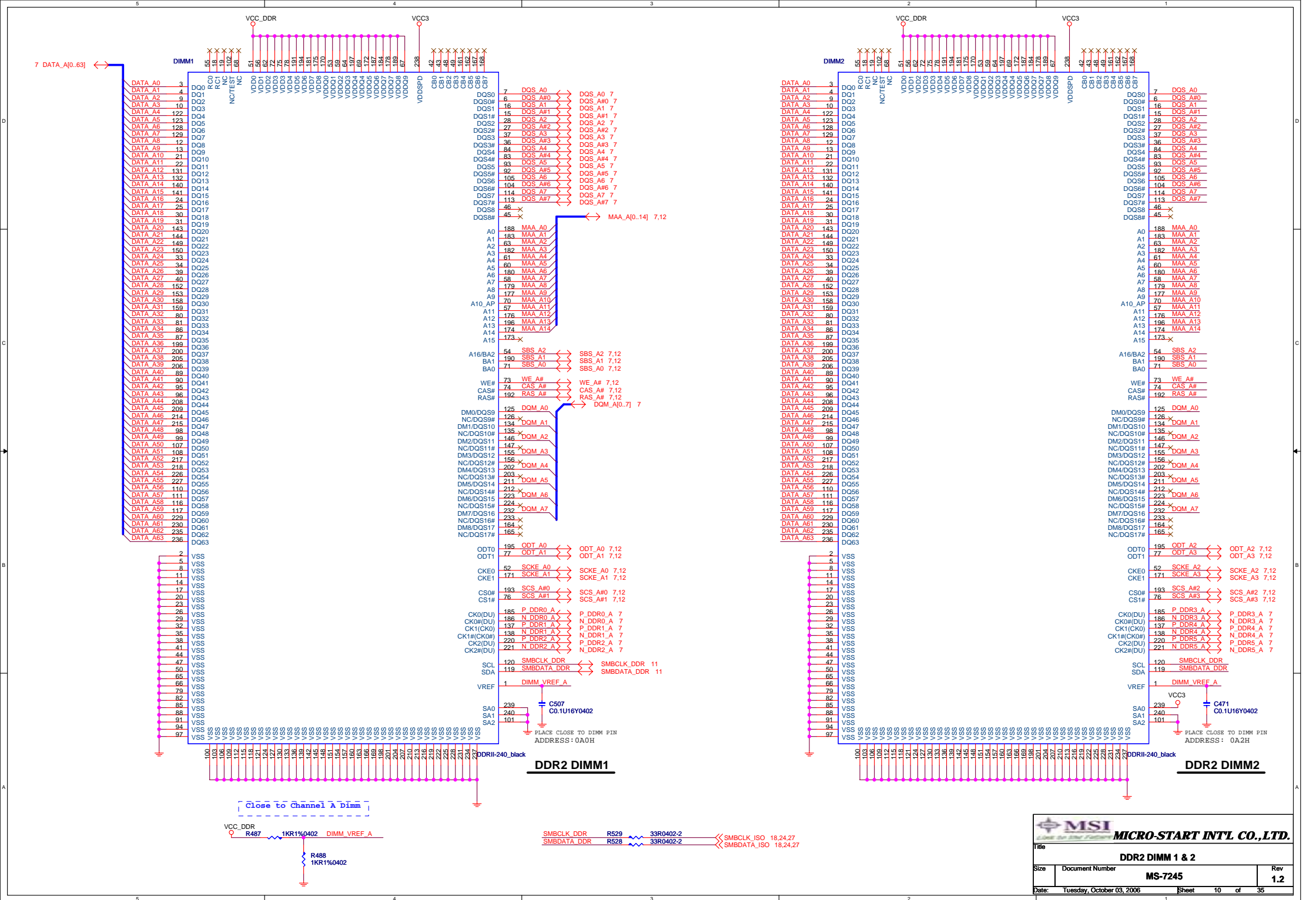
MICRO-START INTL CO.,LTD.		
Title		
INTEL LGA775 POWER		
Size	Document Number	Rev
	MS-7245	1.2
Date:	Tuesday, October 03, 2006	Sheet 4 of 35





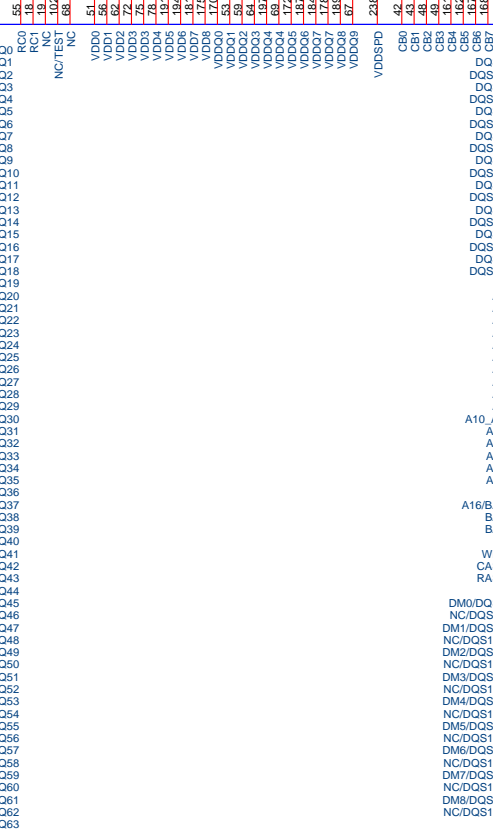




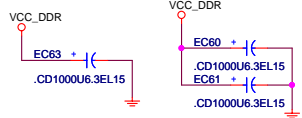
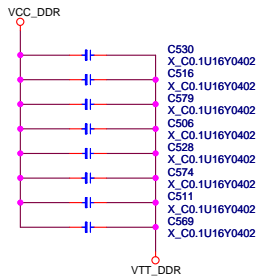
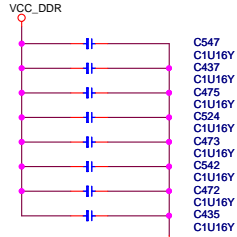
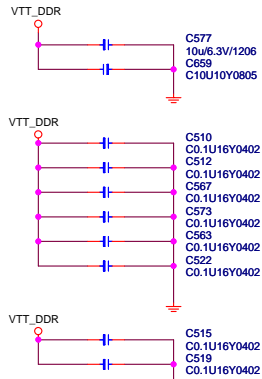


7 DATA_B[0..63]

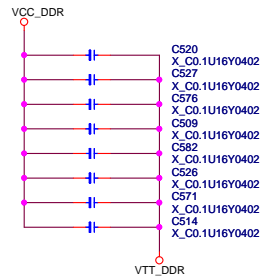
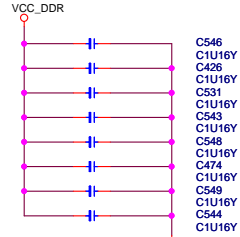
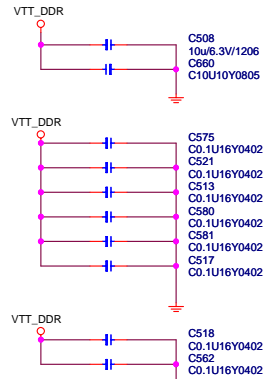
DIMM3



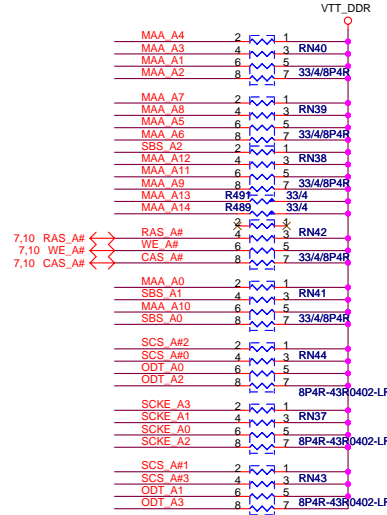
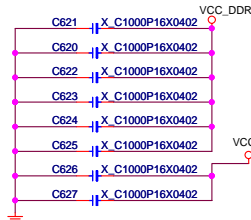
CHANNEL A V_SM_VTT DECOUPLING CAPS



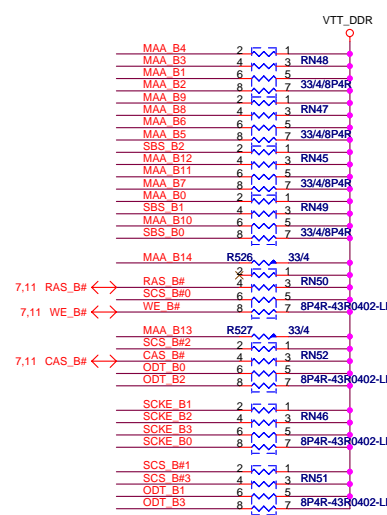
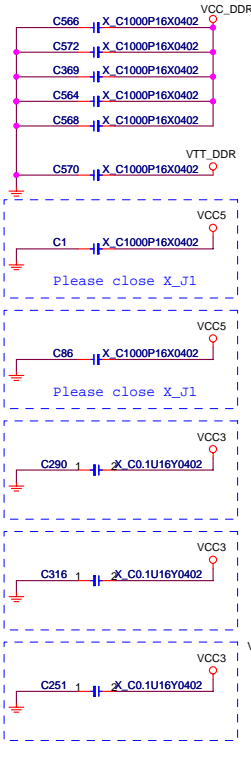
CHANNEL B V_SM_VTT DECOUPLING CAPS



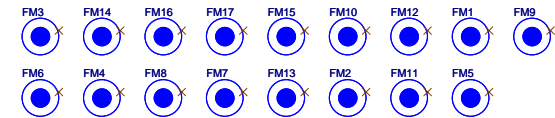
EMI CAPS reserve



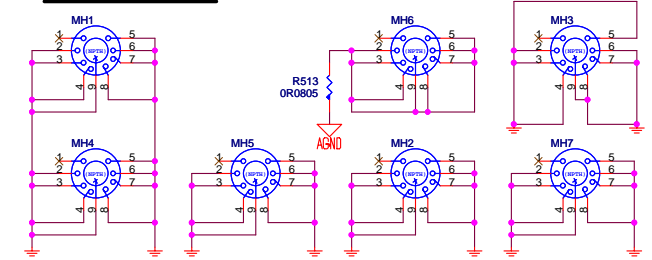
EMI CAPS reserve



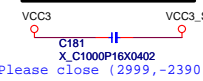
Optical Fiducial Marks



Mounting Holes

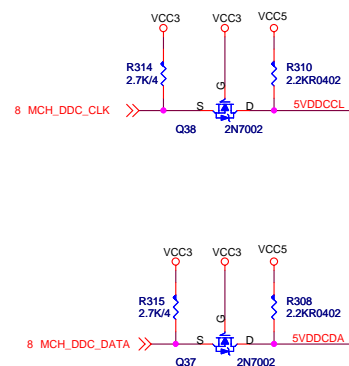
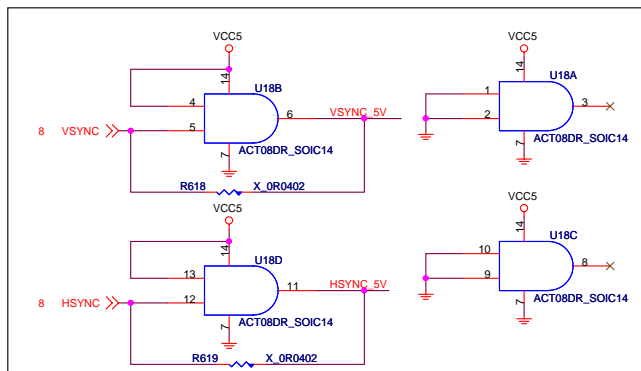
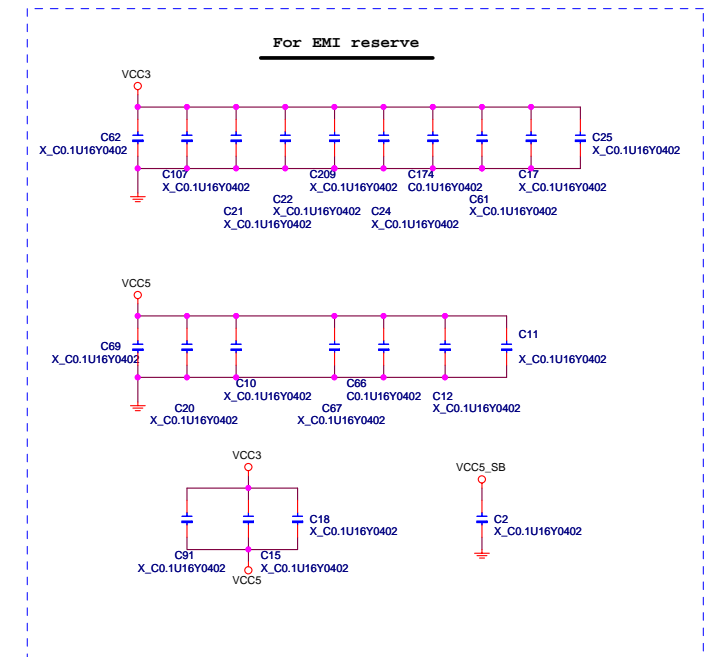
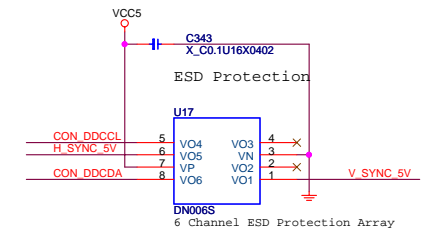
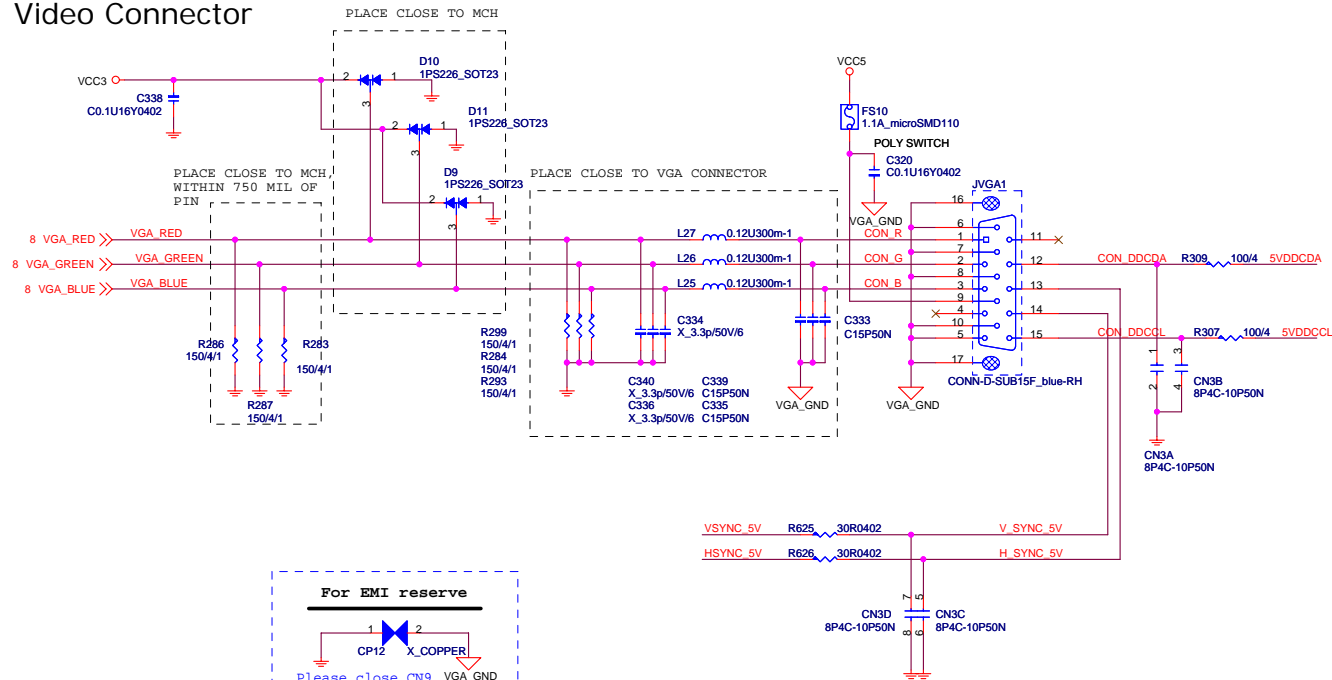


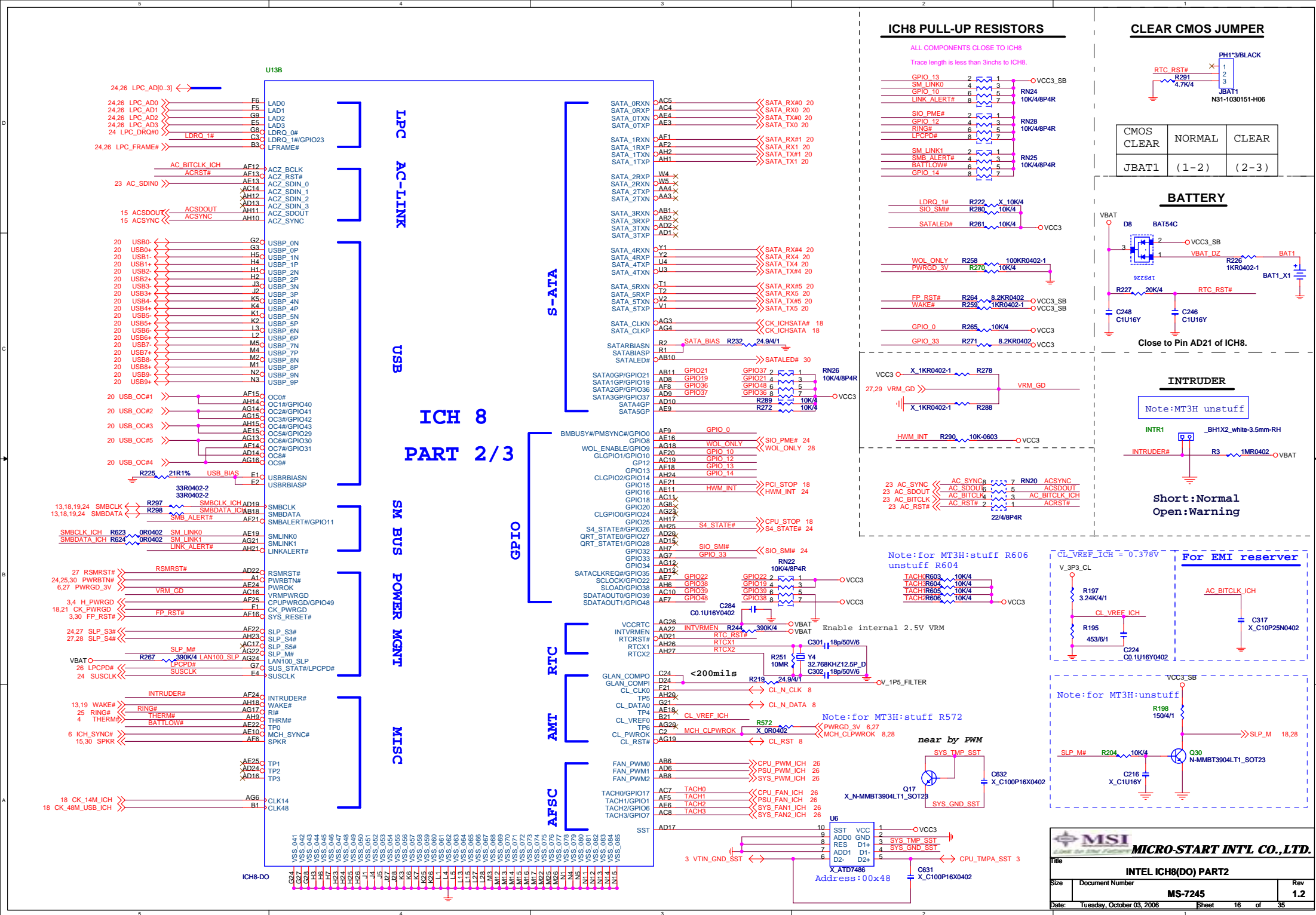
For EMI reserve



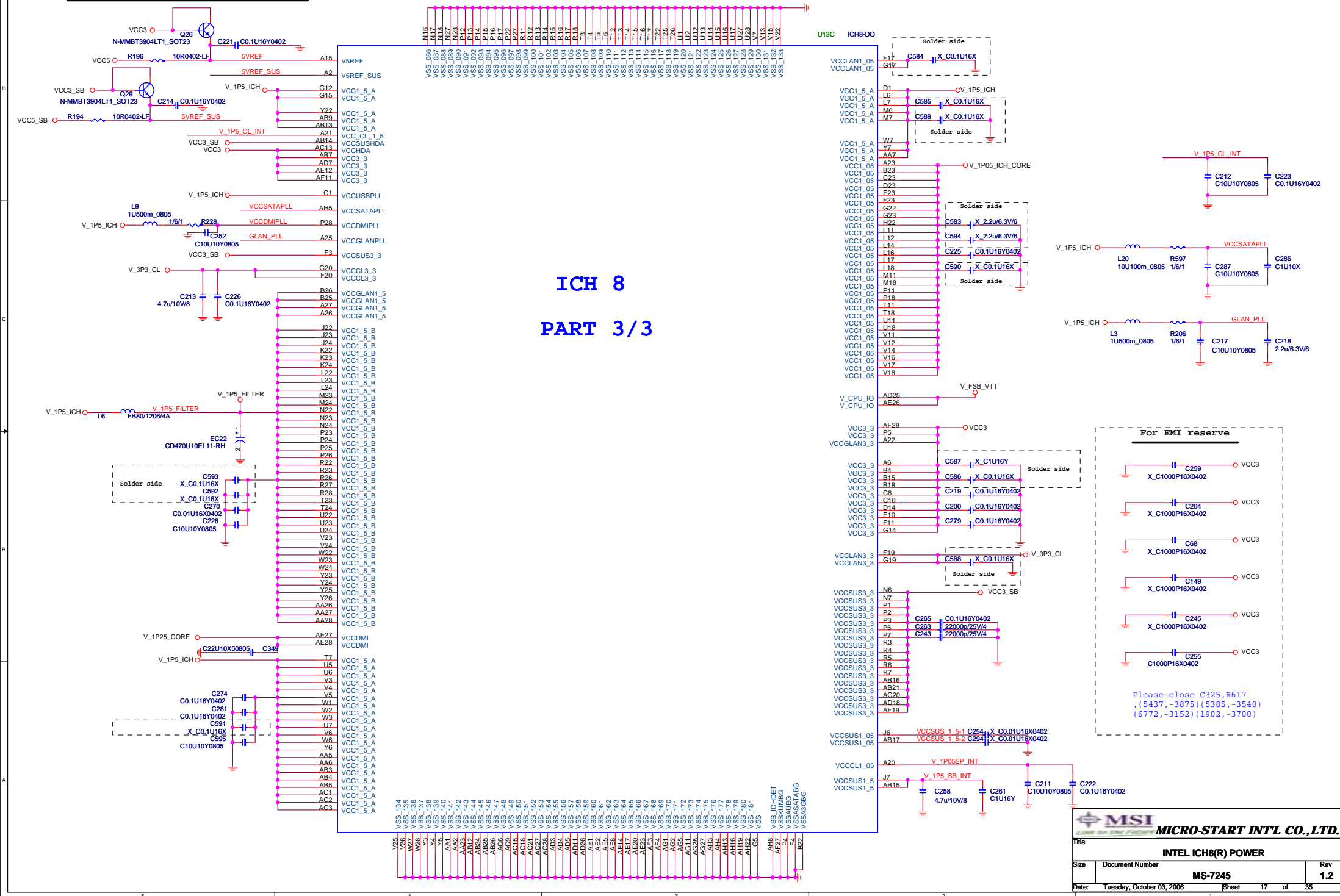
MICRO-START INTL CO.,LTD.		
Title		
DDR TERMINATION		
Size	Document Number	Rev
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Video Connector





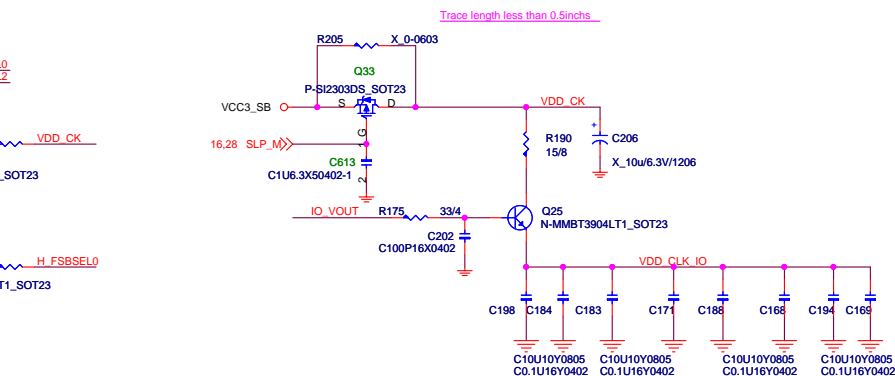
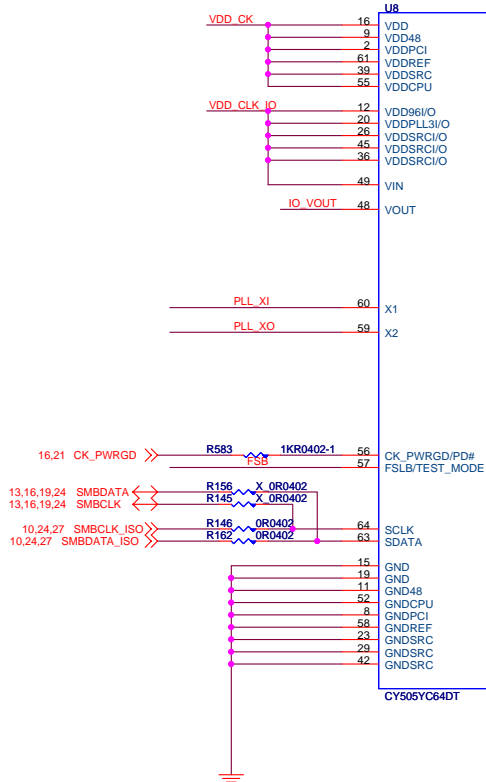
5VREF & 5VREF_SUS Sequencing Circuit



```

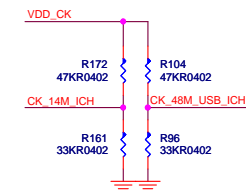
Please put all caps close CLK GEN.

```

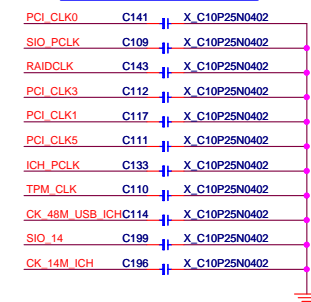


Note:for MT3H
Stuff:R113
Untuff:R124

3,4,8	H_FSBSEL1	H_FSBSEL1	R155	1KR0402-1	FSB
3,4,8	H_FSBSEL0	H_FSBSEL0	R95	X 10K/4	USB 48M
3,4,8	H_FSBSEL2	H_FSBSEL2	R181	X 10K/4	CK_14M



For EMI reserver

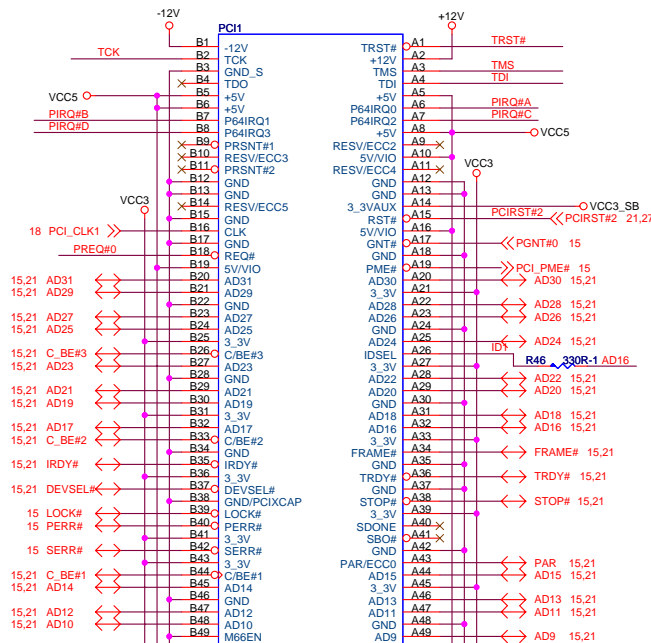


```

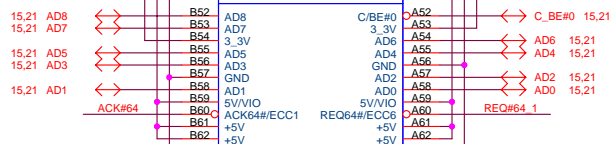
SRC5/SRC5# enable:stuff R113 -
| butput 100MHZ
| CPU_STOP#,PCI_STOP#:stuff R124
| normal input hi,low leave for
| iAMT function.

```

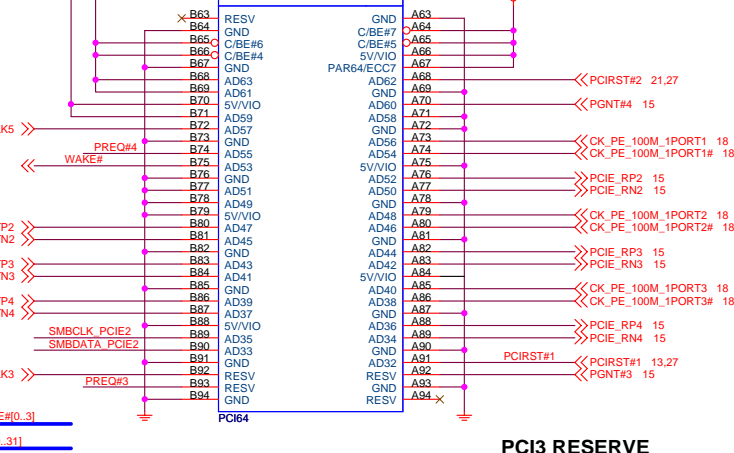
PCI1/PCIEXTENT



KEY



KEY



IDSEL = AD16

MASTER = PREQ#0

PIRQ#A

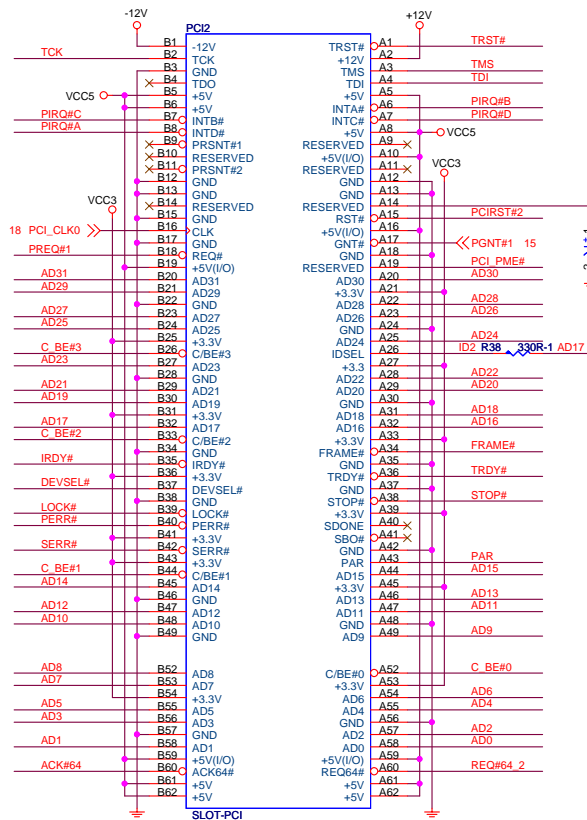
PCI3 RESERVE

IDSEL = AD18

MASTER = PREQ#3

PIRQ#C

PCI SLOT 1 (PCI VER: 2.3 COMPLY)



IDSEL = AD17

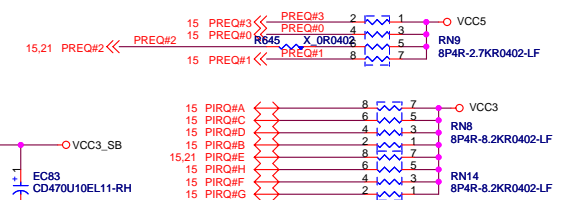
MASTER = PREQ#1

PIRQ#B

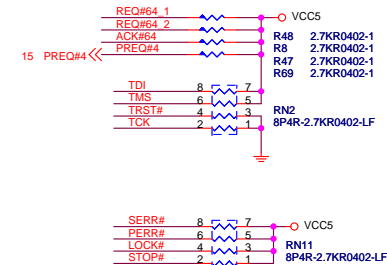
For EMI reserve

+12V C84 X_C0.01U16X0402

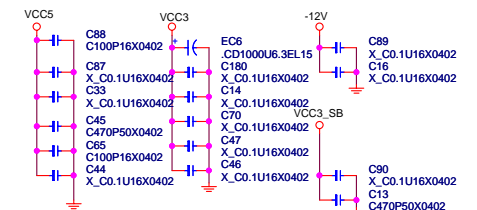
PCI PULL-UP / DOWN RESISTORS



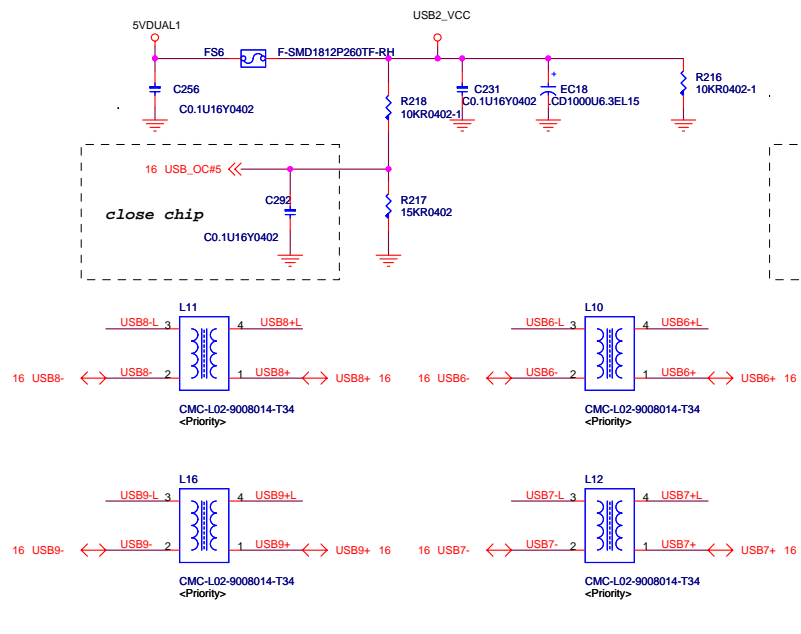
For VIA VT6410 issue



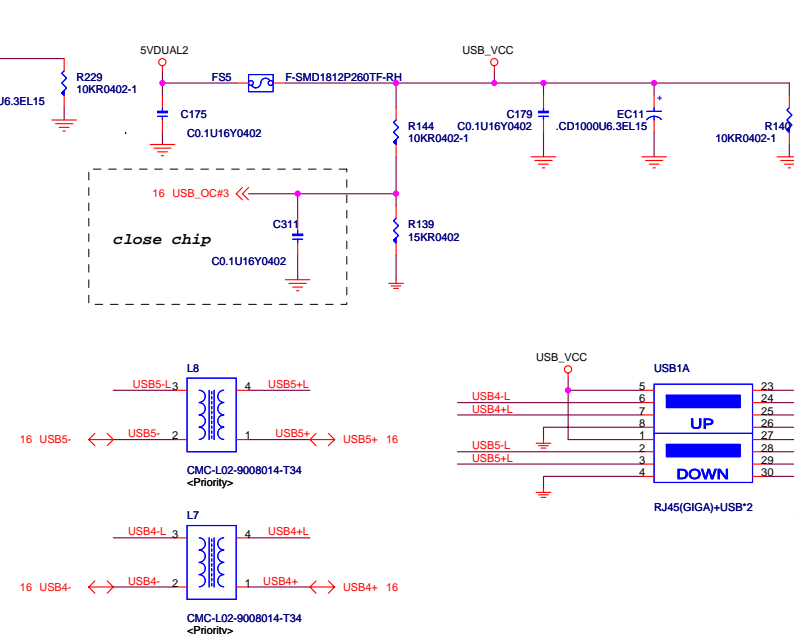
PCI SLOT DECOUPLING CAPACITORS



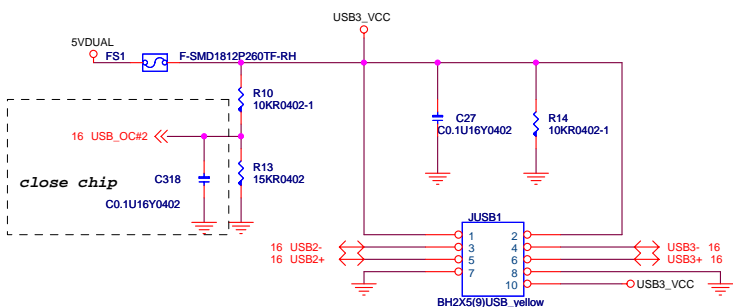
POWER CIRCUIT FOR USB PORT 6,7,8,9 (REAR)



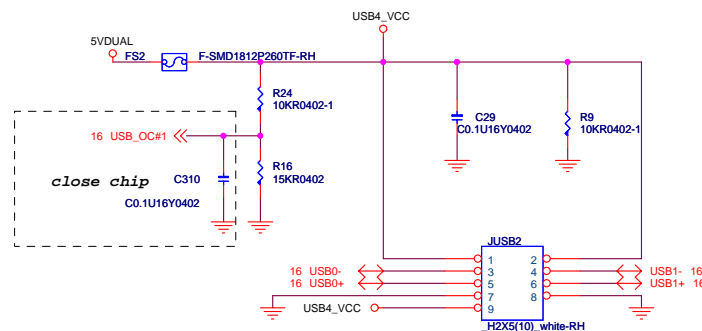
EXTERNAL USB PORT 4,5(REAR)



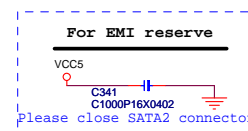
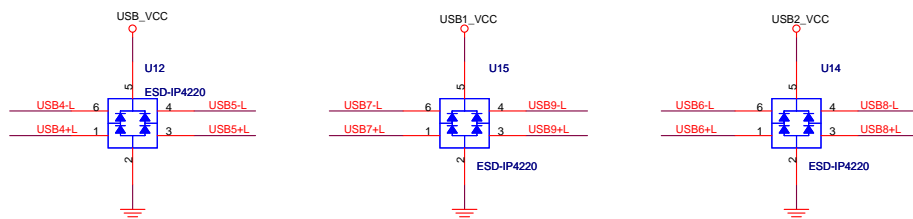
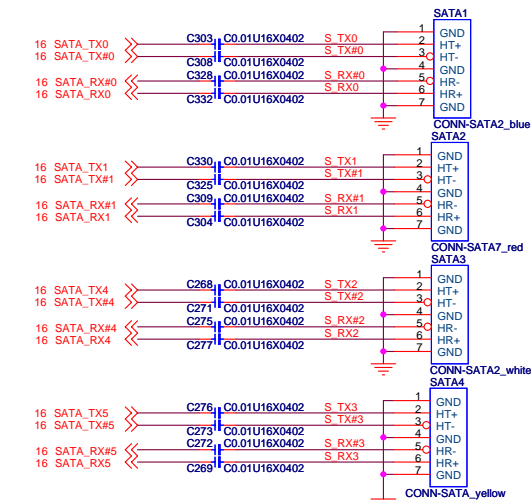
EXTERNAL USB PORT 2,3



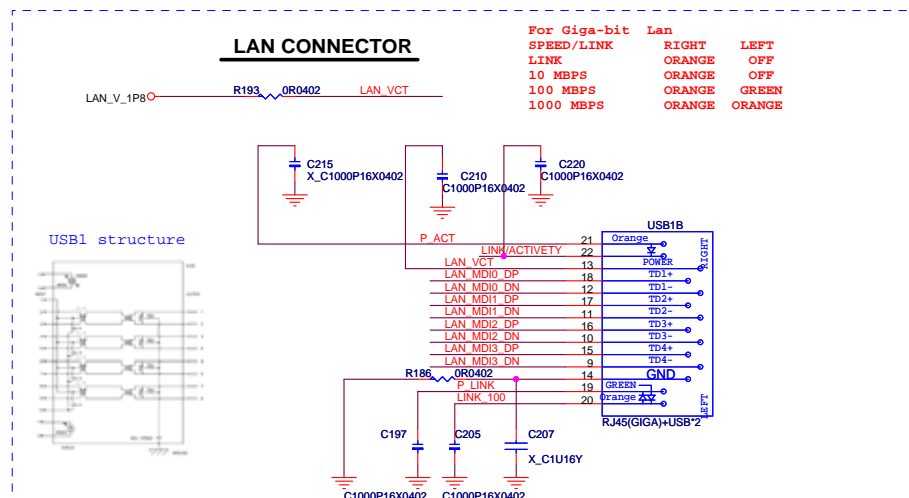
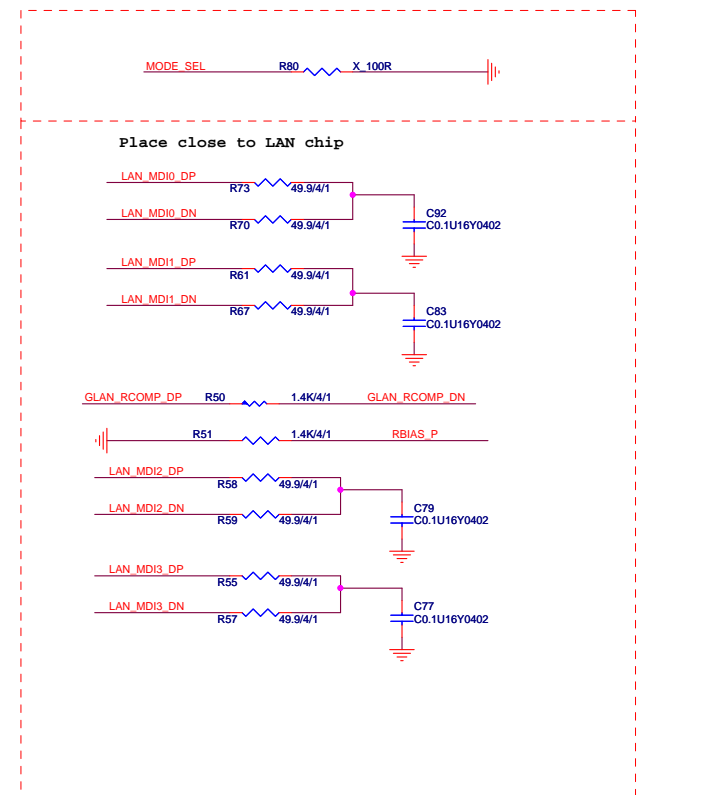
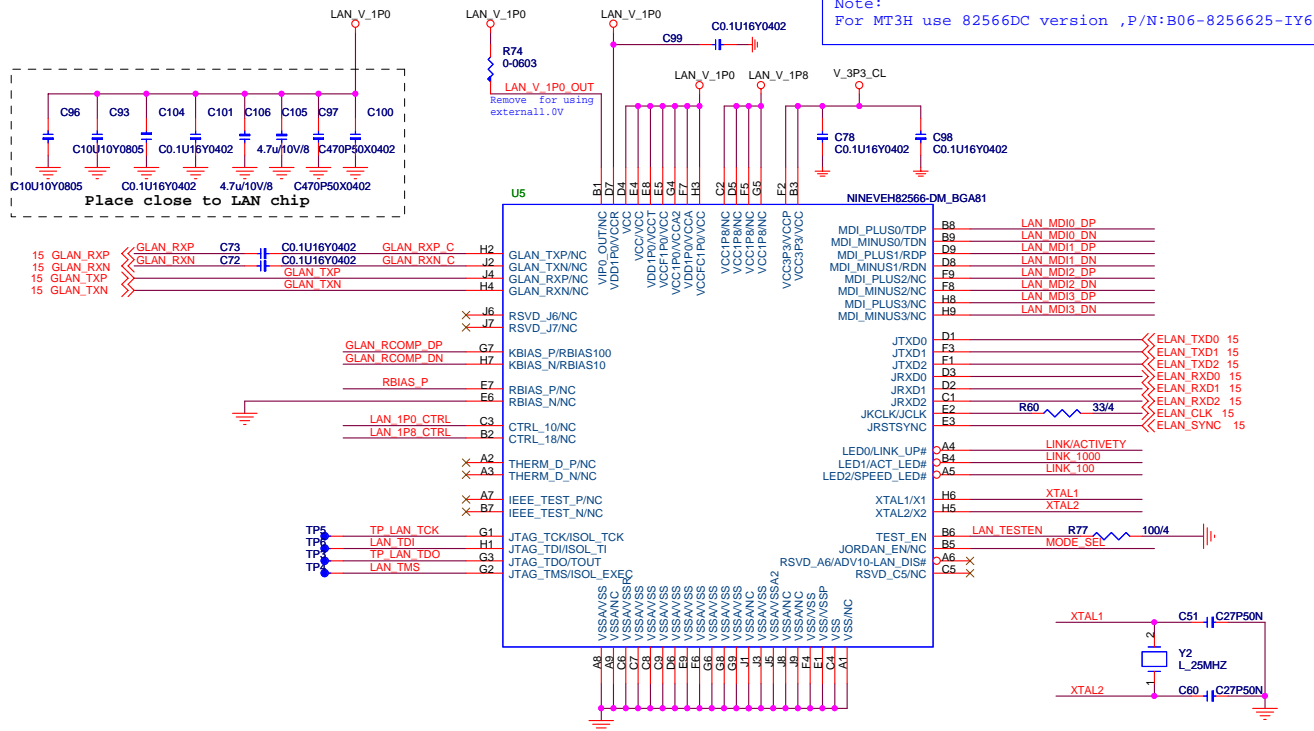
EXTERNAL USB PORT 0,1



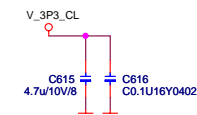
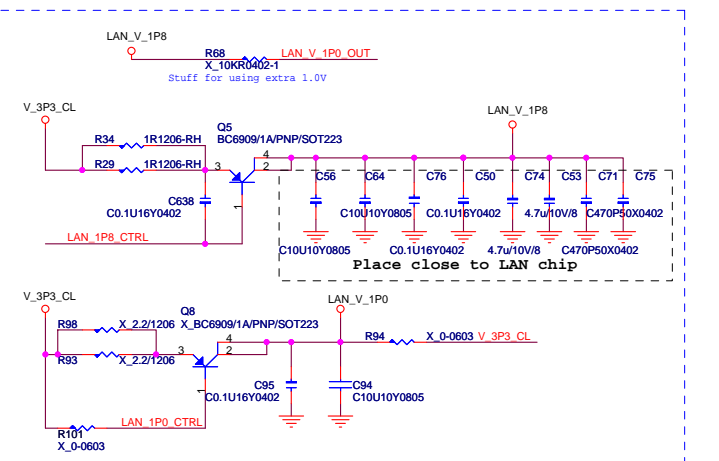
SERIAL ATA CONNECTOR BLOCK



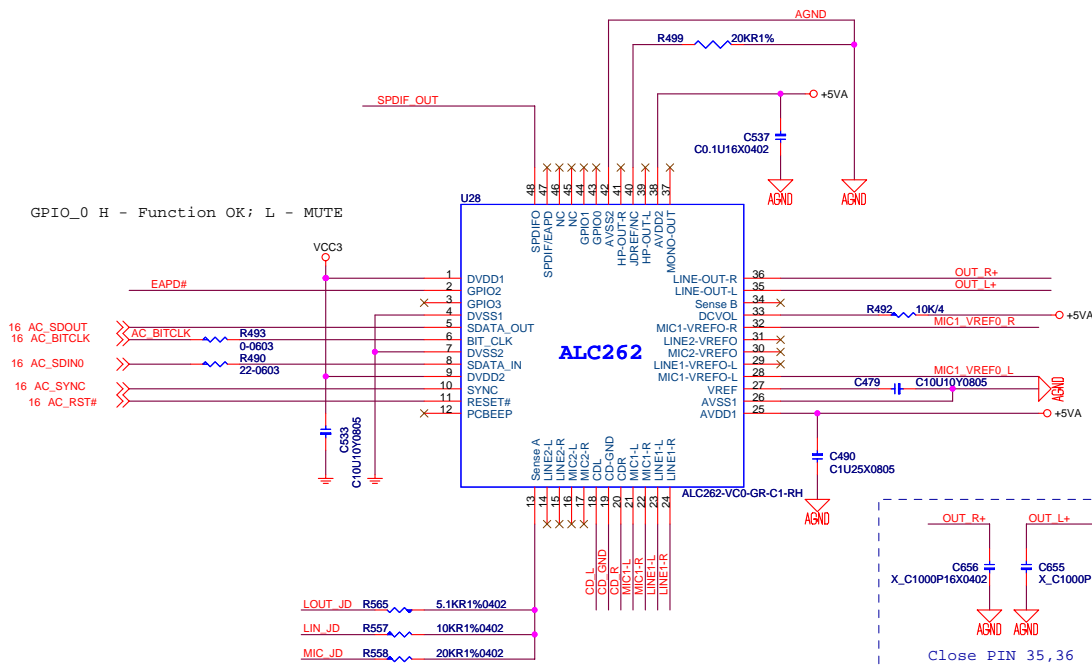
LAN - NINEVEH



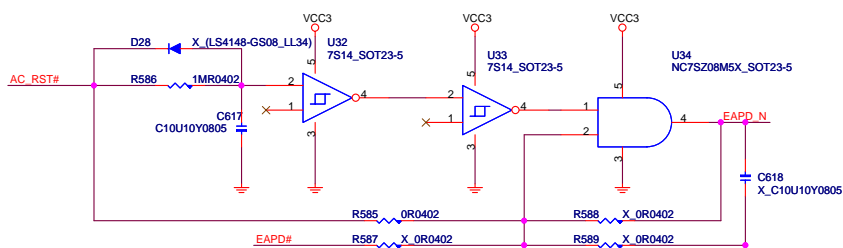
ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH



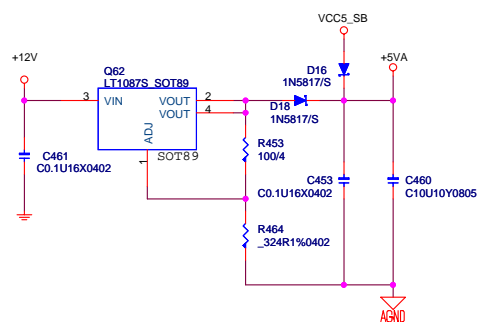
GPIO_0 H - Function OK; L - MUTE



POP noise circuit

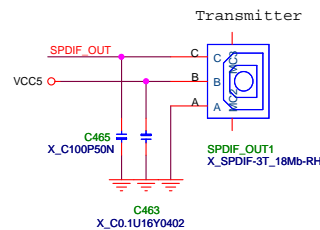


AUDIO CODE REGULATORS



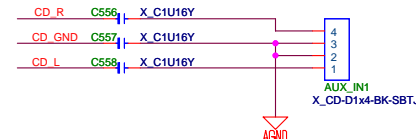
SPDIF OUT

Note:
For MT3H stuff



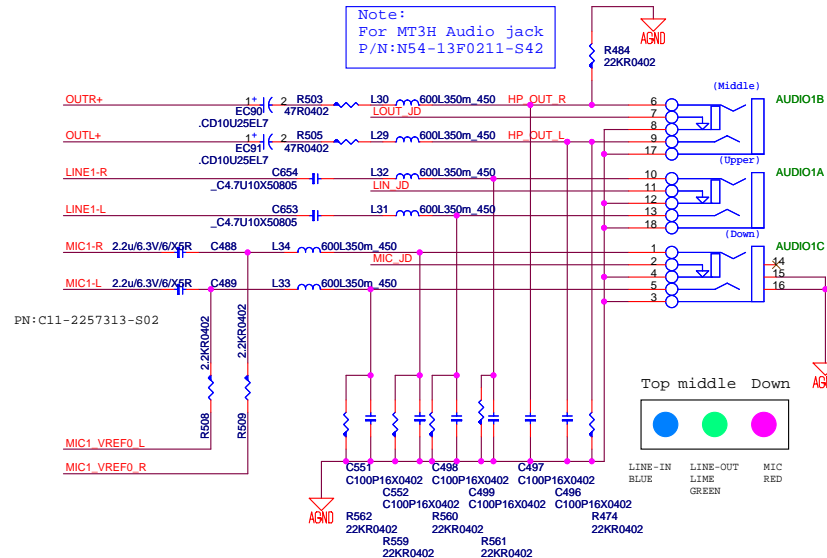
AUX IN

Note:
For MT3H stuff

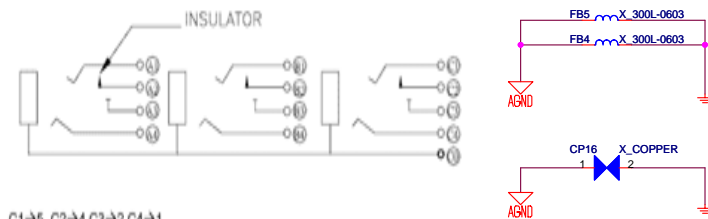


PHONE JACK.

Note:
For MT3H Audio jack
P/N:N54-13F0211-S42

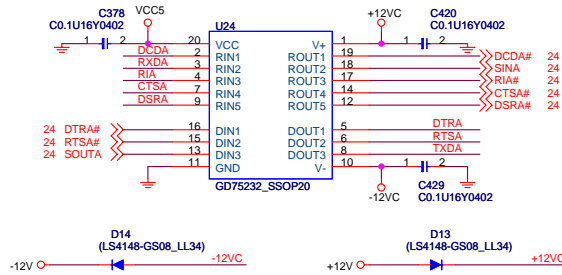


Jack schematic:

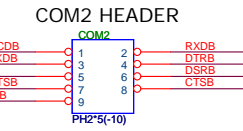
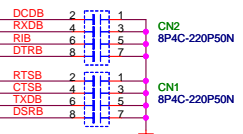
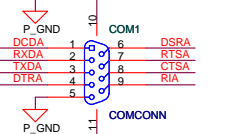
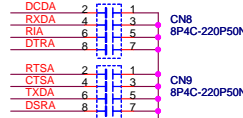
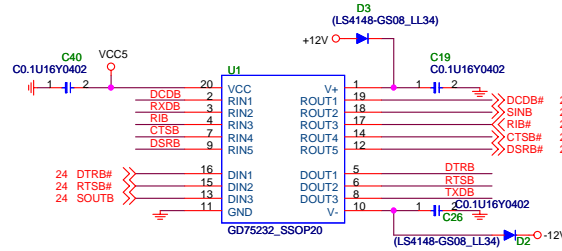


C1→5, C2→4, C3→2, C4→1
B1→9, B2→8, B3→7, B4→6
A1→13, A2→12, A3→11, A4→10
C0→3, 15, 16, 17, 18
Prevent function→14
C→MIC, B→Line out, A→Line in

SERIAL PORT 1

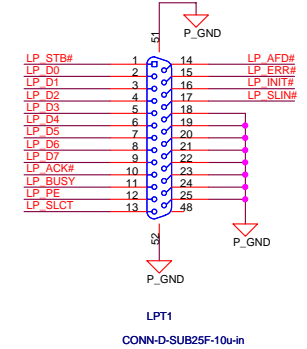
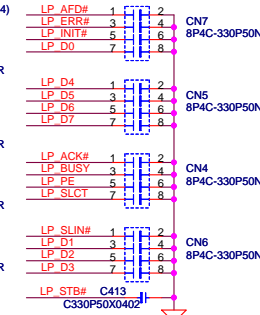
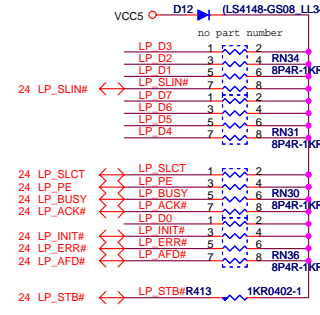


SERIAL PORT 2

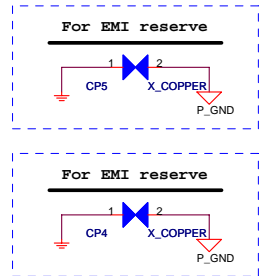


PARALLAL PORT

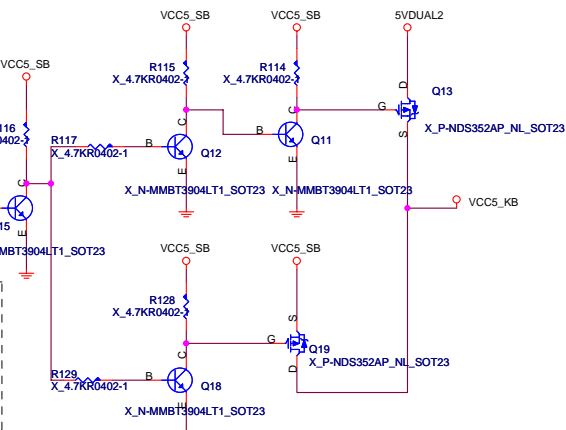
24 LP_D[0..7] ↔ LP D[0..7]



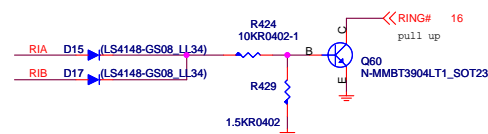
K/B Power supply function for NEC



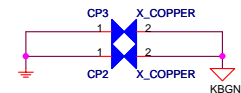
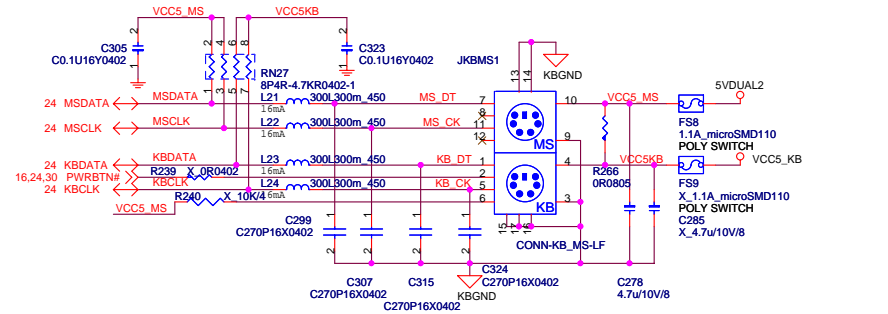
GPIO_KB
HI:VCC5_KB = USB1_VCC
LOW:VCC5_KB = VCC5_SB
VCC DUAL(USB1_VCC)
S0/S1:VCC5
S3:VCC5_SB
S4/S5:0V



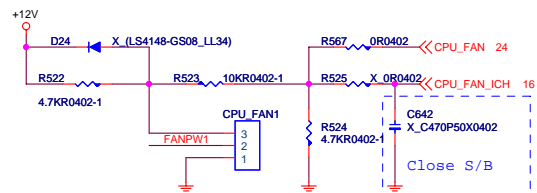
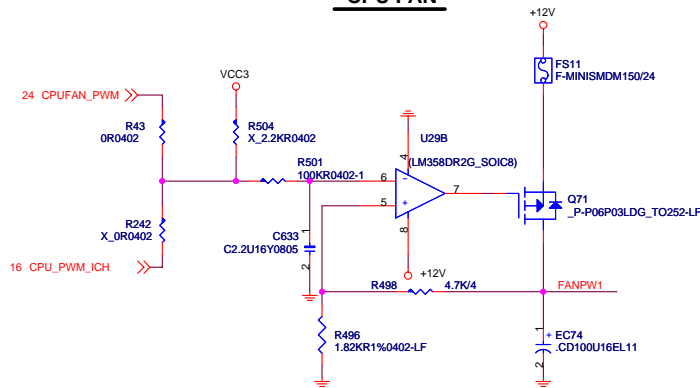
Wake On Modem Header



PS2 KEYBOARD & MOUSE CONNECTOR



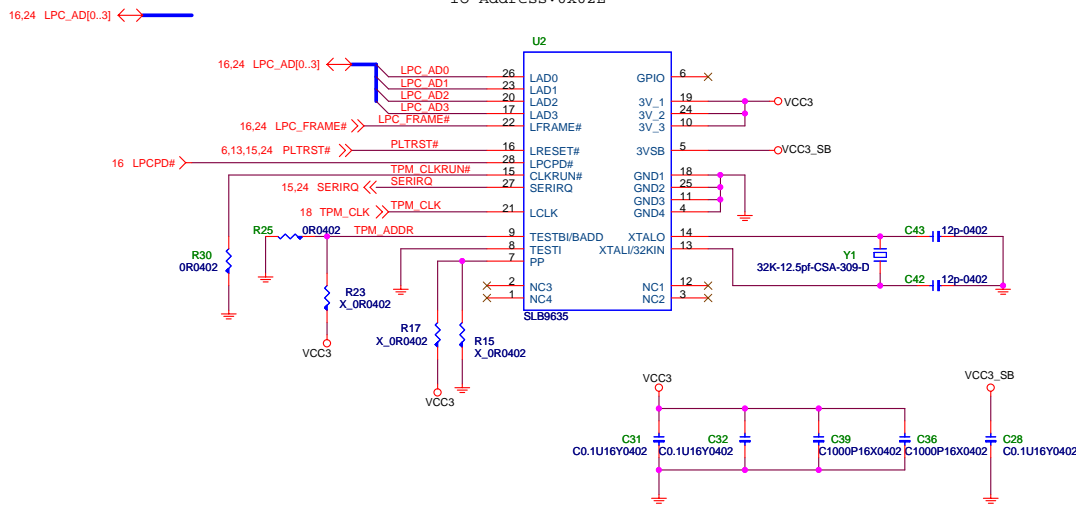
CPU FAN



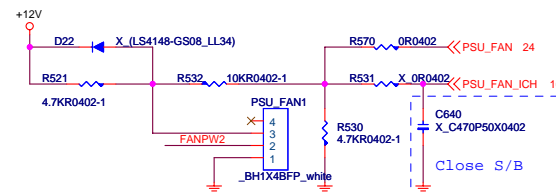
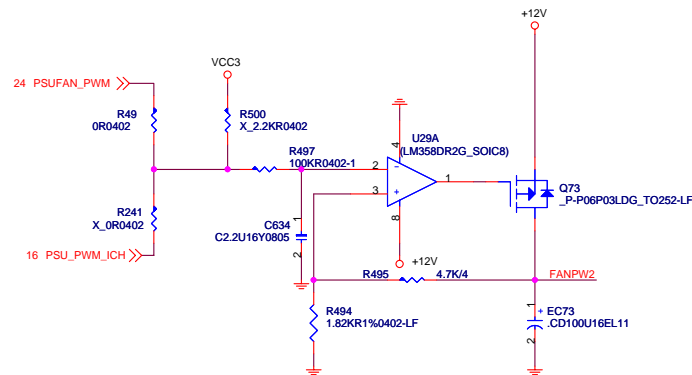
TPM 1.2

Note: MT3H unstuff (plesae see page35)

IO Address:0x02E



PSU FAN



For EMI reserve

VCC5

C346 C0.1U16Y0402

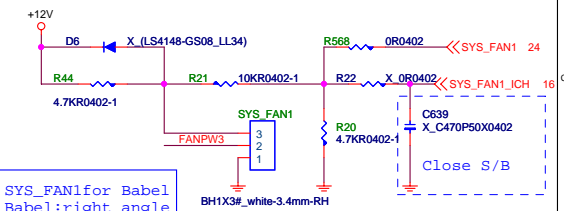
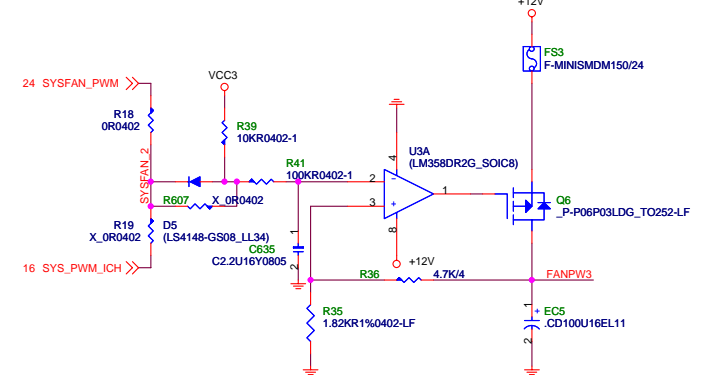
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For EMI reserve

VCC5
C85 X_C0.1U16Y0402

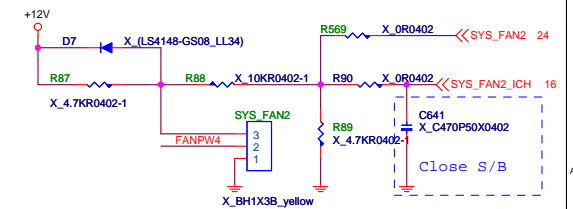
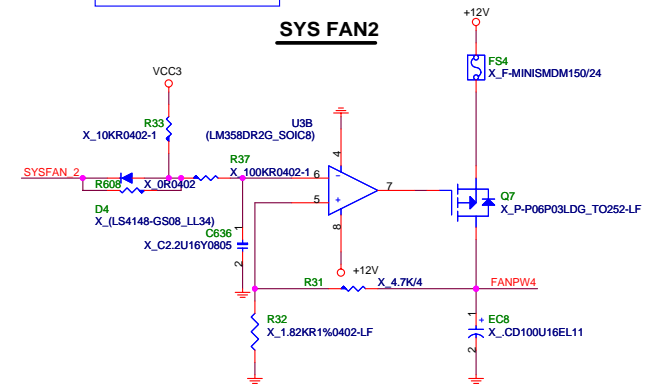
Please close (-2450 5020)

SYS FAN1



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SYS_FAN1for Babel
Babel:right angle
SYS_FAN2 for MT3H
MT3:STD
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SYS FAN2



MICRO-START INTL CO.,LTD.

Title	
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FAN/TPM1.2

Size	Document Number	Rev
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MS-7245

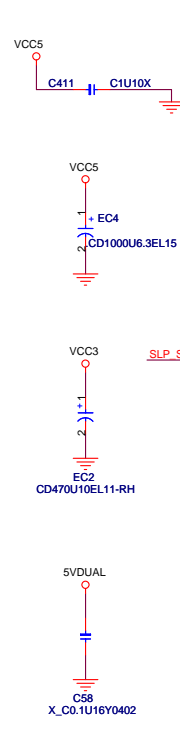
Rev	
1.2	

Date: Tuesday, October 03, 2006 Sheet 26 of 35

	1
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3VSB MODE SELECT	
3VSB MODE	3VDLDEC#
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

[illegible]

Rear USB2

5VUSB DRV

5V DRV

5V DUAL2

5V DUAL1

Q22

Q75

VCC5_SB C177

R534

X_0R1206

X_1N8977S

D26

VCC5

N-IPD06N03LAG_T0252

5V DRV 2

5V DRV 1

5V USB DRV

R550 10K/4

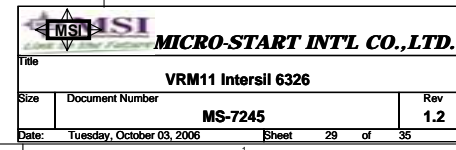
C065 1U10X

NN-P07D03LV_S08

SOT23

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[illegible]



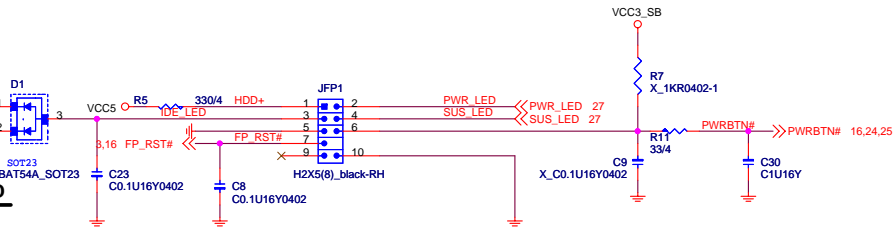
Front Panel

IDE LED

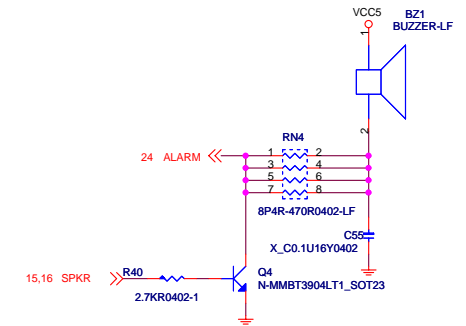
21 IDEACTP# >>
Active-low

Active-low
16 SATALED# >>

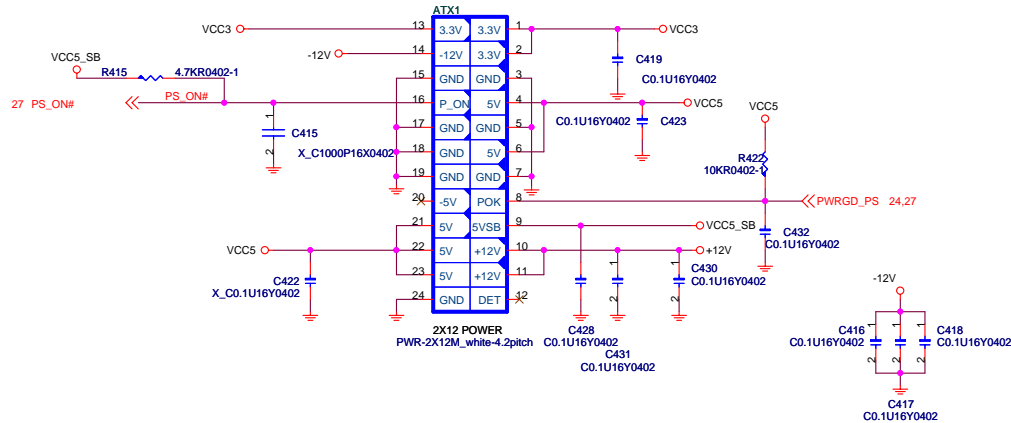
SERIAL ATA LED



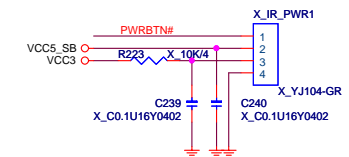
SPEAKER



ATX Connector



For NEC IR POWER



ICH8

GPIO Pin	Type	Default	Function	Power	MUXED/ UNMUXED	Pin-out
GPIO 0	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AF9
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AF5
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 10K	VCC3		D5
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 10K	VCC3		F10
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 10K	VCC3		G11
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 10K	VCC3		F9
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AE6
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AC8
GPIO 8	I/O	GPI	SIO_PME# connect to SIO,pull_up VCC3_SB with 10k	VCC3_SB	UNMUXED	AE16
GPIO 9	I/O	MGPIO3	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AG18
GPIO 10	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AF20
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		AF21
GPIO 12	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VBT	UNMUXED	AC19
GPIO 13	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	UNMUXED	AF18
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AH24
GPIO 15	I/O	GPO	PCI_STOP	VCC3_SB	UNMUXED	AE21
GPIO 16	I/O	GPO	SIO HWM_INT,pull_up VCC3 with 10K(change to GPI)		UNMUXED	AE11
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AC7
GPIO 18	I/O	GPO	NC		UNMUXED	AC11
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AD8
GPIO 20	I/O	GPO	NC		UNMUXED	AG8
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AB11
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AE7
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull_up VCC3 with 10K	VCC3	MUXED	C3
GPIO 24	I/O	GPO	NC		MUXED	AG23
GPIO 25	I/O	GPO	CPU_STOP	3.3V_SB	UNMUXED	AH17
GPIO 26	I/O	GPO	S4 STATE			AH25
GPIO 27	I/O	GPO	NC	3.3V_SB		AD20
GPIO 28	I/O	GPO	NC			AD15
GPIO 29	I/O	OC5#	OC#3 connect to USB connector	3.3V_SB		AE15
GPIO 30	I/O	OC6#	OC#4 connect to USB connector	3.3V_SB		AG13
GPIO 31	I/O	OC7#	OC#4 connect to USB connector	3.3V_SB		AF14
GPIO 32	I/O	GPO	SIO_SMI# connect to SIO,pull up VCC3 with 10k	VCC3	UNMUXED	AH7
GPIO 33	I/O	GPO	Pull-up to VCC3 with 8.2K		UNMUXED	AG7
GPIO 34	I/O	GPO	NC		UNMUXED	AG12
GPIO 35	I/O	GPO	NC			AD12
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF8
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD9
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH6
GPIO 39	I/O	GPI	Pull-down to GND with 10K directly	VCC3		AC10
GPIO 40	I/O	OC1#	OC#1 connect to USB connector	VCC3		AH14
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	VCC3		AG14
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	VCC3		AG15
GPIO 43	I/O	OC4#	OC#3 connect to USB connector	VCC3		AH15
GPIO 48	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF7
GPIO 49	I/O	CPU_PWRGD	H_PWRGD connect to CPU	VTT_OUT		AF25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 10K	VCC5	MUXED	C16
GPIO 51	I/O	GNT1#	GNT1#		MUXED	A15
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC5 with 10K	VCC5	MUXED	B16
GPIO 53	I/O	GNT2#	GNT2#		MUXED	D17
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 10K	VCC5	MUXED	A9
GPIO 55	I/O	GNT3#	GNT3#		MUXED	B9

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI1 EXTENT	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK1
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK0
VT6410	PIRQ#E	PREQ#2 PGNT#2	AD20	RAIDCLK
PCI3	RESERVED	PREQ#3 PGNT#3	AD18	PCI_CLK3

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	SCLK_A0/SCLK_A0# SCLK_A1/SCLK_A1# SCLK_A2/SCLK_A2#
DIMM 2	0A2H	SCLK_A3/SCLK_A3# SCLK_A4/SCLK_A4# SCLK_A5/SCLK_A5#
DIMM 3	0A4H	SCLK_B0/SCLK_B0# SCLK_B1/SCLK_B1# SCLK_B2/SCLK_B2#
DIMM 4	0A6H	SCLK_B3/SCLK_B3# SCLK_B4/SCLK_B4# SCLK_B5/SCLK_B5#

SIO SCH5017

PIN NAME	PIN#	USAGE	Input/Output
GP43	92	GPIO_KB	OUTPUT
GP27	36	SIO_SMI#	OUTPUT
GP42	90	SIO_PME#	OUTPUT
INTRD_IN~	33	CLEAR_PASSWORD	INPUT

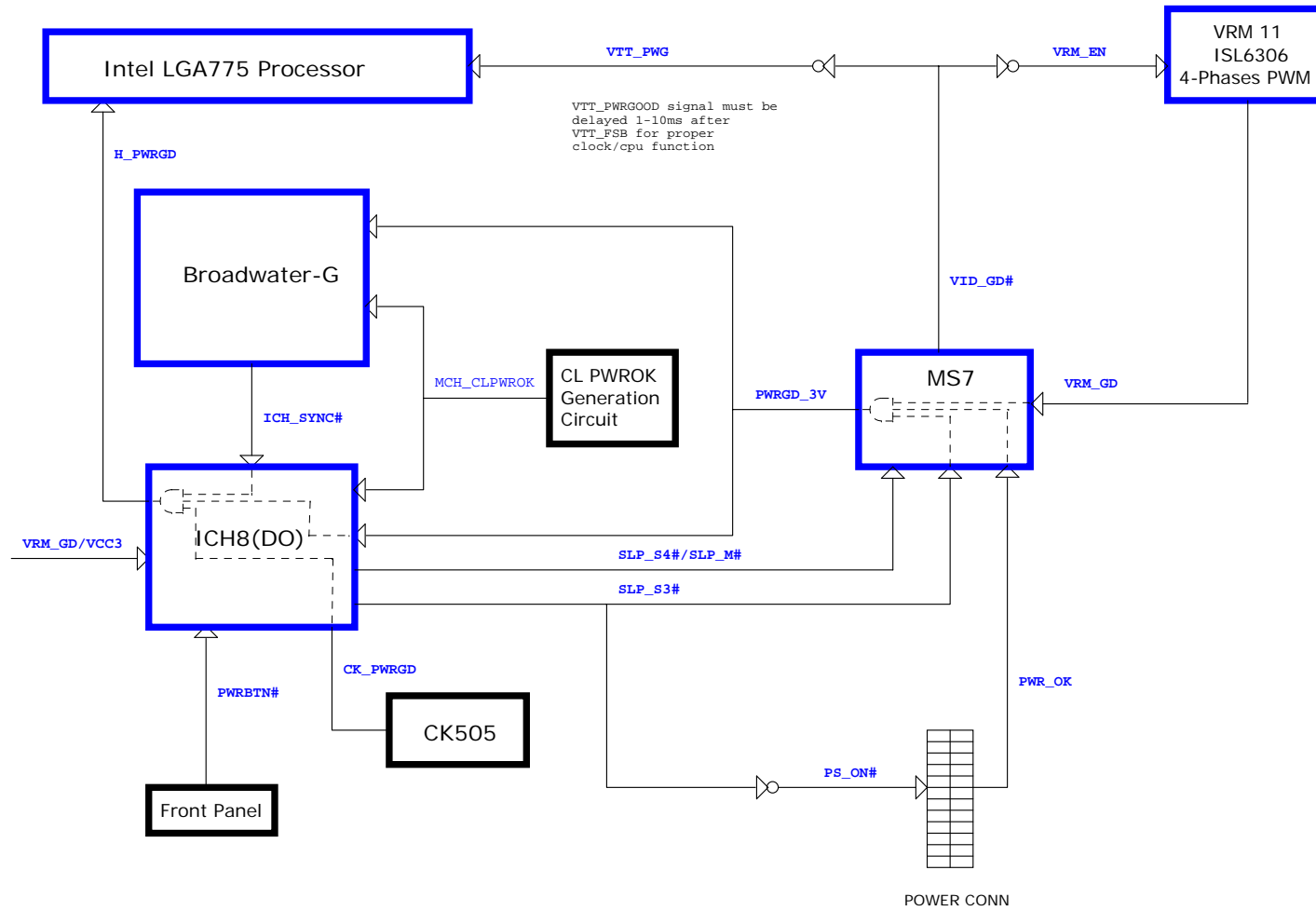
SMBus DISTRIBUTION

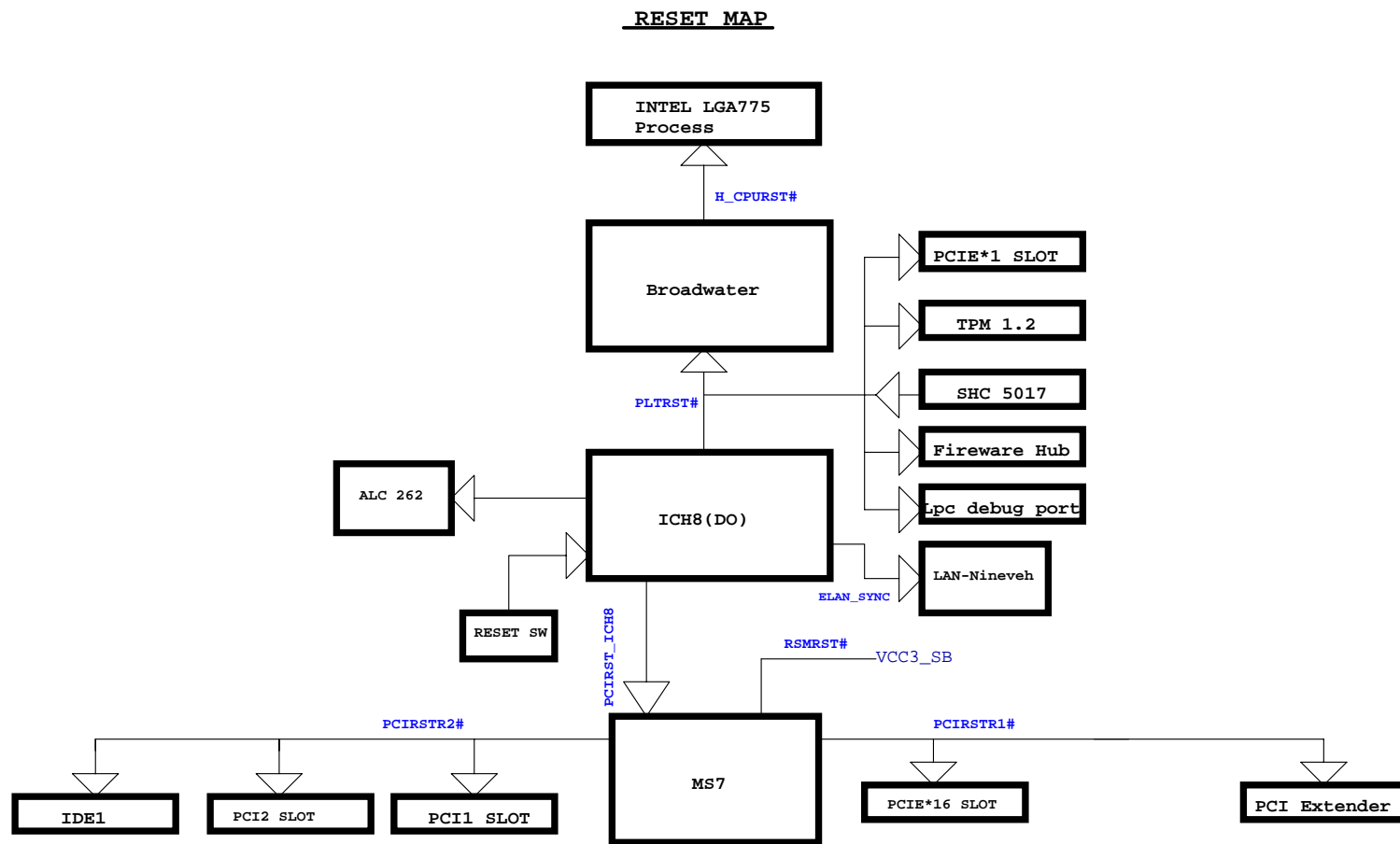
SMBus	Power	Load
SMBCLK	VCC3_SB	ICH8, SIO,PCI EXPRESS x16,x1
SMBCLK_ISO	VCC3	DIMM, CLK GEN, SIO, MS7,LAN

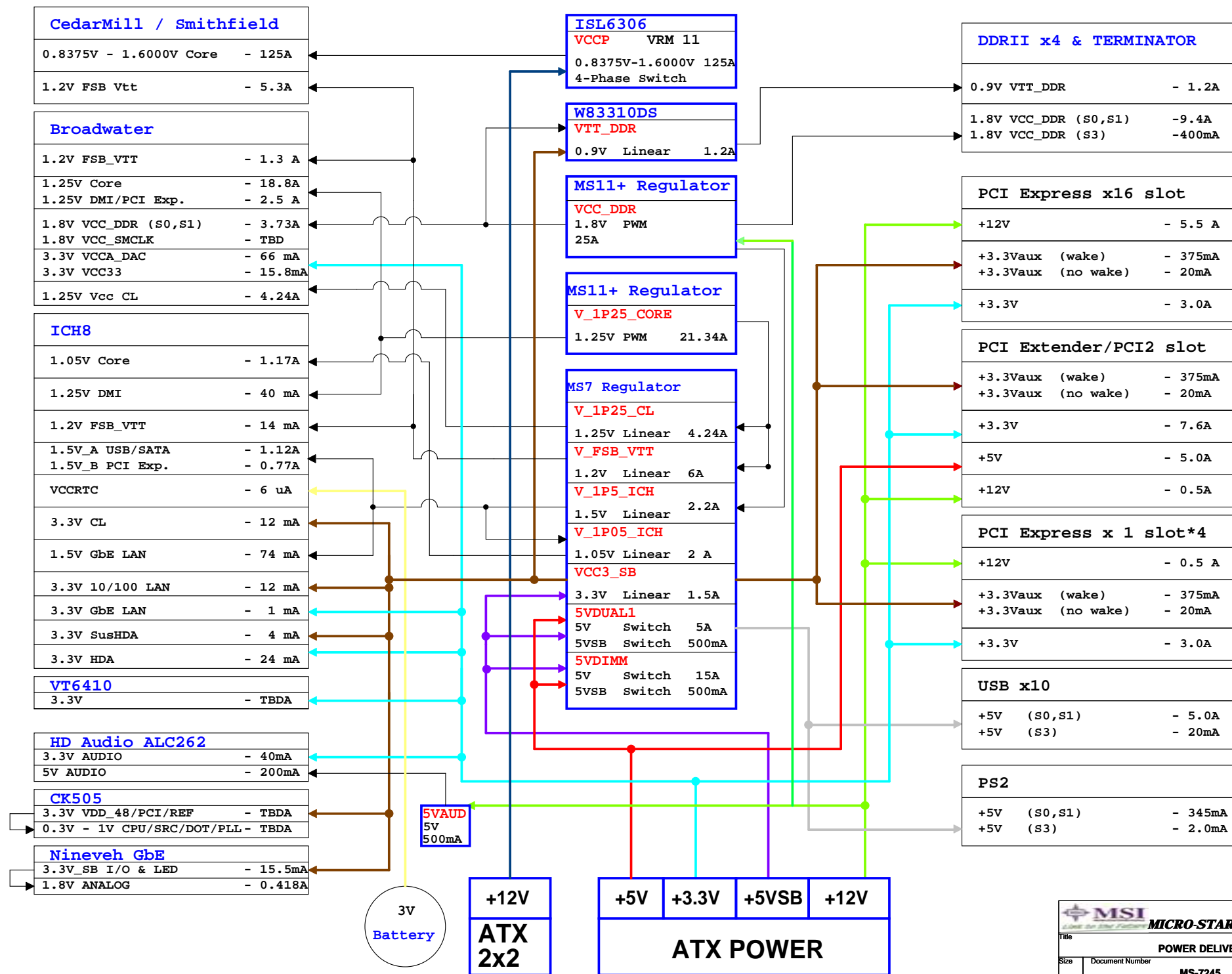
JUMPER SETTING

JBAT1	(1-2)Normal	(2-3)Clear
INTRUDER	Short Normal	Open warning
JFWD1	(1-2) open clear	(1-2)short Normal

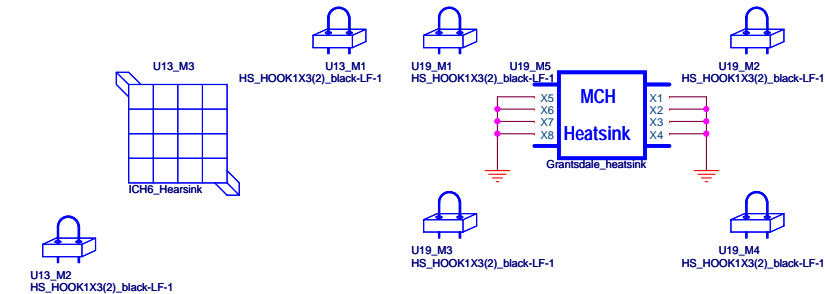
PWROK MAP







COMMON MANUAL PART



MT3H MANUAL PART

